

MEMORY

CMOS

MASK ROM CARD

PCMCIA Rel.2/JEIDA Ver.4 conformable

MB98A51121/51221/51321/51421/51521-17

MASK ROM CARD 2 M/4 M/8 M/16 M/32 M-BYTE

■ DESCRIPTION

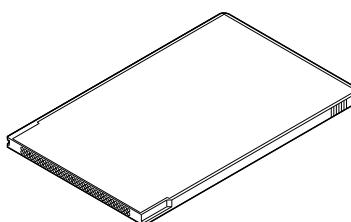
This card is a PCMCIA and JEIDA-compliant 68-pin two-piece Mask ROM card with the 16-bit mask ROM being installed on the common memory.

However, to use this card as PCMCIA Rel.2, JEIDA Ver.4, the card attribute information has to be stored in the Mask ROM.

■ FEATURES

- External dimensions: 85.6 mm × 54.0 mm × 3.3 mm
- +5 V single power supply
- Usable in 8 bits × 16 bits configuration
- Complete static operation
- I/O level TTL compatible
- Output tri-state
- Complete capacitive load without pull-up resistor or pull-down resistor except \overline{CE}_1 and \overline{CE}_2 .
- 68-pin two-piece connector form

■ PACKAGE



(CRD-68P-M04)

MB98A51121/51221/51321/51421/51521-17

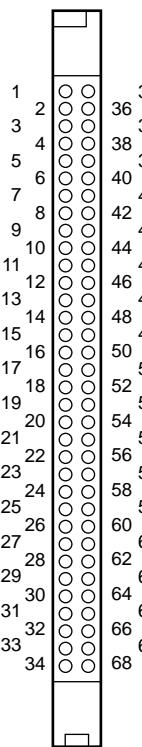
■ PRODUCT CLASS

| Part Number | Memory Device | Memory Configuration (word × bit) | Access Time (ns) (max.) |
|-------------|---------------------------|--------------------------------------|-------------------------|
| MB98A51121 | 16-Mbit Mask ROM ×1 pcs | 2 M × 8/1 M × 16 | 170 |
| MB98A51221 | 16-Mbit Mask ROM × 2 pcs | 4 M × 8/2 M × 16 | |
| MB98A51321 | 16-Mbit Mask ROM × 4 pcs | 8 M × 8/4 M × 16 | |
| MB98A51421 | 16-Mbit Mask ROM × 8 pcs | 16 M × 8/8 M × 16 | |
| MB98A51521 | 16-Mbit Mask ROM × 16 pcs | 32 M × 8/16 M × 16 | |

MB98A51121/51221/51321/51421/51521-17

■ PIN ASSIGNMENTS

(CONNECTOR SIDE)



(CRD-68P-M02)

- Pin Name

| Symbol | I/O | Pin Name |
|-------------------------------------|-----|-------------------------------|
| A ₀ to A ₂₅ | I | Address input |
| D ₀ to D ₁₅ | I/O | Data I/O |
| CE ₁ , CE ₂ | I | Card enable |
| CD ₁ , CD ₂ * | O | Card detection |
| VS ₁ , VS ₂ | O | Voltage sense |
| REG | I | Attribute memory space select |
| OE | I | Output enable |
| WE | I | Write enable |
| BVD1, BVD2 * | O | Battery voltage detection |
| WP * | O | Write protect |
| V _{CC} | — | Supply voltage (+5 V) |
| GND | — | Ground |
| N.C. | — | No connection |

* : Those pins are internally connected; use care when handling.

| Pin No. | Symbol | Pin No. | Symbol |
|---------|-----------------|---------|-------------------------|
| 1 | GND | 35 | GND |
| 2 | D ₃ | 36 | CD ₁ |
| 3 | D ₄ | 37 | D ₁₁ |
| 4 | D ₅ | 38 | D ₁₂ |
| 5 | D ₆ | 39 | D ₁₃ |
| 6 | D ₇ | 40 | D ₁₄ |
| 7 | CE ₁ | 41 | D ₁₅ |
| 8 | A ₁₀ | 42 | CE ₂ |
| 9 | OE | 43 | VS ₁ * |
| 10 | A ₁₁ | 44 | N.C. |
| 11 | A ₉ | 45 | N.C. |
| 12 | A ₈ | 46 | A ₁₇ |
| 13 | A ₁₃ | 47 | A ₁₈ |
| 14 | A ₁₄ | 48 | A ₁₉ * |
| 15 | WE/N.C. * | 49 | A ₂₀ * |
| 16 | N.C. | 50 | A ₂₁ /N.C. * |
| 17 | V _{CC} | 51 | V _{CC} |
| 18 | N.C. | 52 | N.C. |
| 19 | A ₁₆ | 53 | A ₂₂ /N.C. * |
| 20 | A ₁₅ | 54 | A ₂₃ /N.C. * |
| 21 | A ₁₂ | 55 | A ₂₄ /N.C. * |
| 22 | A ₇ | 56 | A ₂₅ /N.C. * |
| 23 | A ₆ | 57 | VS ₂ * |
| 24 | A ₅ | 58 | N.C. |
| 25 | A ₄ | 59 | N.C. |
| 26 | A ₃ | 60 | N.C. |
| 27 | A ₂ | 61 | REG/N.C. * |
| 28 | A ₁ | 62 | BVD2 |
| 29 | A ₀ | 63 | BVD1 |
| 30 | D ₀ | 64 | D ₈ |
| 31 | D ₁ | 65 | D ₉ |
| 32 | D ₂ | 66 | D ₁₀ |
| 33 | WP | 67 | CD ₂ |
| 34 | GND | 68 | GND |

* : Whether a pin is an address pin or N.C. pin depends on the type of the models. See ■ DIFFERENCE OF PIN FUNCTIONS.

MB98A51121/51221/51321/51421/51521-17

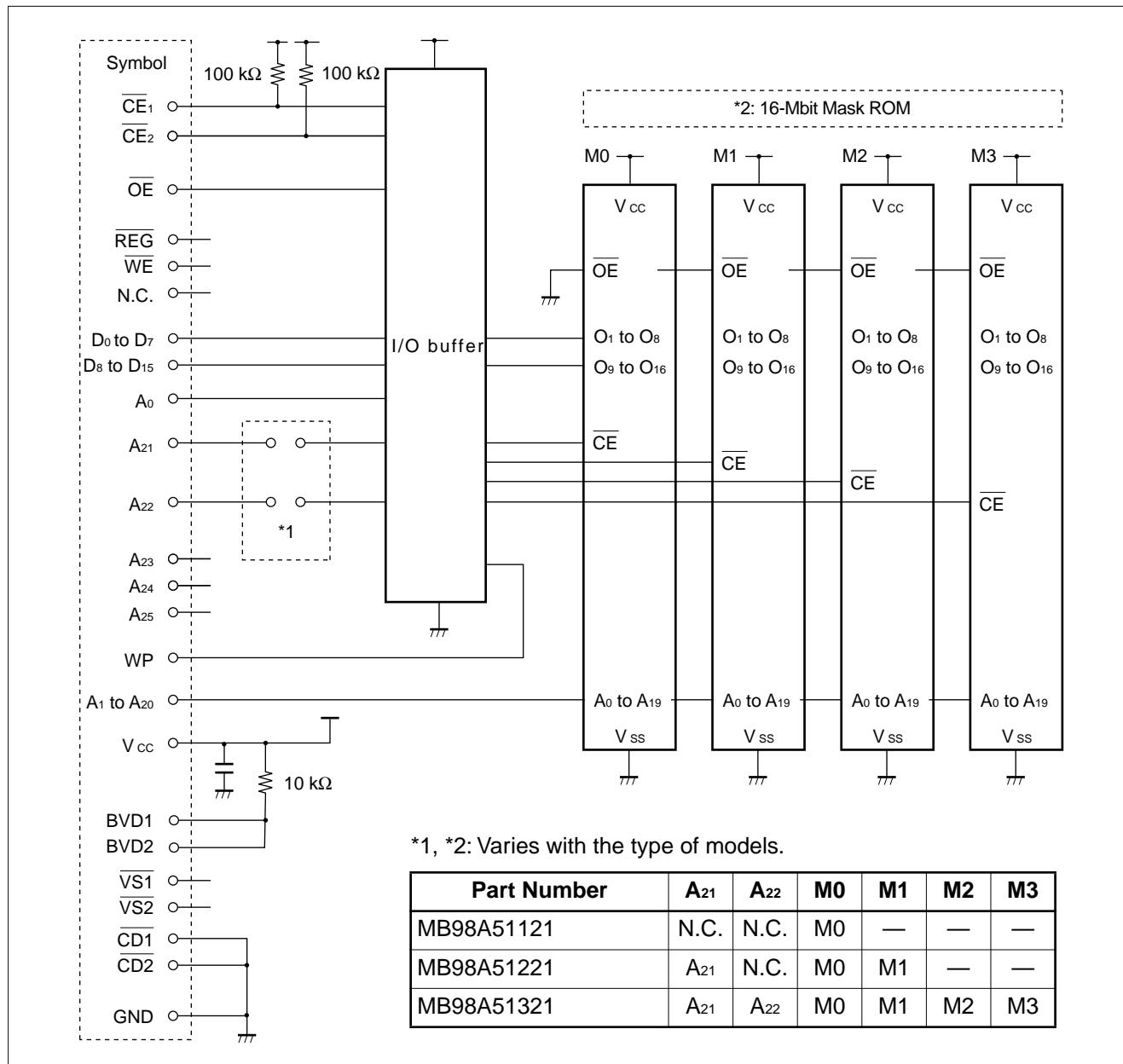
■ DIFFERENCE OF PIN FUNCTIONS

| Part Name | A ₂₁ | A ₂₂ | A ₂₃ | A ₂₄ | A ₂₅ | REG | WE | VS ₁ | VS ₂ |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------|-----------------|-----------------|
| MB98A51121 | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. |
| MB98A51221 | | | | | | | | | |
| MB98A51321 | | | | | | | | | |
| MB98A51421 | | | | | | | | | |
| MB98A51521 | A ₂₁ | A ₂₂ | A ₂₃ | A ₂₄ | | | | | |

MB98A51121/51221/51321/51421/51521-17

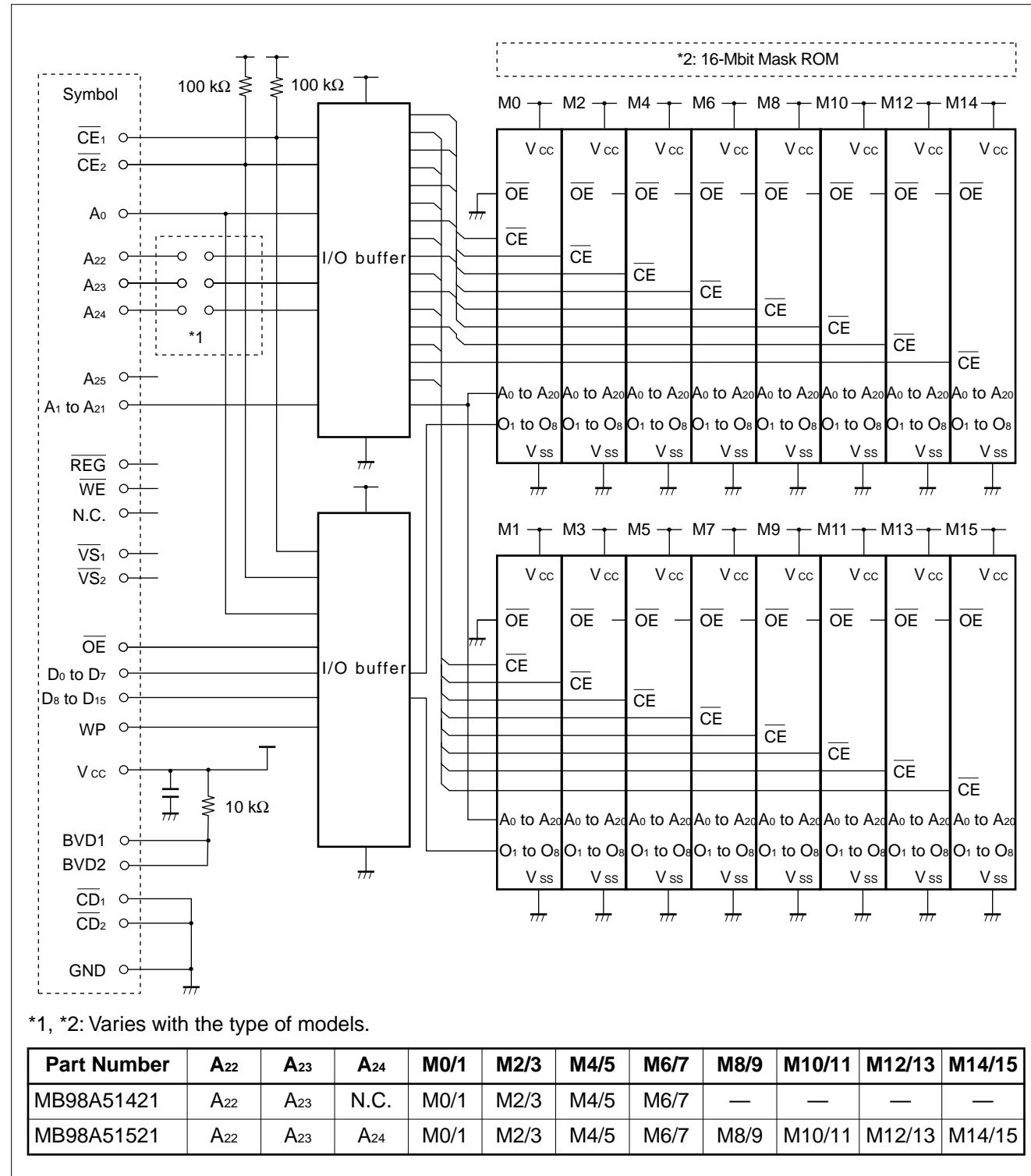
■ BLOCK DIAGRAM

1. 16-Mbit Mask ROM $\times 1/ \times 2/ \times 4$ Being Mounted



MB98A51121/51221/51321/51421/51521-17

2. 16-Mbit Mask ROM $\times 8 \times 16$



*1, *2: Varies with the type of models.

| Part Number | A ₂₂ | A ₂₃ | A ₂₄ | M0/1 | M2/3 | M4/5 | M6/7 | M8/9 | M10/11 | M12/13 | M14/15 |
|-------------|-----------------|-----------------|-----------------|------|------|------|------|------|--------|--------|--------|
| MB98A51421 | A ₂₂ | A ₂₃ | N.C. | M0/1 | M2/3 | M4/5 | M6/7 | — | — | — | — |
| MB98A51521 | A ₂₂ | A ₂₃ | A ₂₄ | M0/1 | M2/3 | M4/5 | M6/7 | M8/9 | M10/11 | M12/13 | M14/15 |

MB98A51121/51221/51321/51421/51521-17**■ FUNCTIONAL TRUTH TABLE**

| CE₂ | CE₁ | A₀ (BYTE) | OE | Operating Mode | Output Pin (D₈ to D₁₅) | Output Pin (D₀ to D₇) |
|-----------------------|-----------------------|---------------------------------|-----------|-----------------------|---|--|
| H | H | × | × | Standby | High-impedance | High-impedance |
| × | × | × | H | Output disable | High-impedance | High-impedance |
| H | L | L | L | Read (× 8 bit) | High-impedance | Output data (even bytes) |
| H | L | H | L | Read (× 8 bit) | High-impedance | Output data (odd bytes) |
| L | H | × | L | Read (× 8 bit) | Output data (odd bytes) | High-impedance |
| L | L | × | L | Read (× 16 bit) | Output data (odd bytes) | Output data (even bytes) |

H: High level, L: Low level, ×: Don't care

MB98A51121/51221/51321/51421/51521-17

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | | Unit |
|---------------------|------------------|-------|-----------------------|------|
| | | Max. | Min. | |
| Supply Voltage * | V _{CC} | -0.3 | +6.0 | V |
| Input Voltage * | V _{IN} | -0.3 | V _{CC} + 0.3 | V |
| Output Voltage * | V _{OUT} | -0.3 | V _{CC} + 0.3 | V |
| Ambient Temperature | T _A | -10 | +60 | °C |
| Storage Temperature | T _{STG} | -30 | +70 | °C |

* : The voltage values are with reference to GND = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|----------------------------|-----------------|-------|------|-----------------------|------|
| | | Min. | Typ. | Max. | |
| Supply Voltage * | V _{CC} | 4.75 | 5.0 | 5.25 | V |
| | GND | — | 0 | — | V |
| High Level Input Voltage * | V _{IH} | 2.4 | — | V _{CC} + 0.3 | V |
| Low Level Input Voltage * | V _{IL} | -0.3 | — | 0.8 | V |
| Ambient Temperature | T _A | 0 | — | +55 | °C |

* : The voltage values are with reference to the GND = 0 V.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(On the recommended conditions)

| Parameter | Notes | Symbol | Test Conditions | Value | | | Unit |
|------------------------------------|-------|------------------|---|-------|-----------|------|---------------|
| | | | | Min. | Typ. | Max. | |
| Standby Supply Current | | I _{SB1} | $\overline{CE}_1, \overline{CE}_2 \geq V_{CC} - 0.2 \text{ V}$ $I_{OUT} = 0 \text{ mA}$ | — | 10 | 1600 | μA |
| | | I _{SB2} | $\overline{CE}_1, \overline{CE}_2 = V_{IH}$ $I_{OUT} = 0 \text{ mA}$ | — | — | 10 | mA |
| Averaging Operation Supply Current | | I _{CC} | Cycle = min. Duty cycle = 100% $I_{OUT} = 0 \text{ mA}, \overline{OE} = V_{IH}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | — | — | 220 | mA |
| Input Leak Current | *1 | I _{LI} | $V_{IN} = 0 \text{ V to } V_{CC}$ | -40 | ± 0.1 | 40 | μA |
| Output Leak Current | *2 | I _{LO} | $V_{OUT} = 0 \text{ V to } V_{CC}$, $\overline{CE}_1, \overline{CE}_2 = V_{IH} \text{ or } \overline{OE} = V_{IH}$ | -10 | — | 10 | μA |
| High Level Output Voltage | *2 | V _{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | — | — | V |
| Low Level Output Voltage | *2 | V _{OL} | $I_{OL} = 2.1 \text{ mA}$ | — | — | 0.4 | V |

Notes: *1. Excluding \overline{CE}_1 and \overline{CE}_2 pins.*2. Excluding WP, BVD1, BVD2, \overline{CD}_1 and \overline{CD}_2 pins.

2. AC Characteristics

(1) Common Memory read cycle

(On the recommended conditions)

| Parameter | Notes | Symbol | Test Conditions | Value | | Unit |
|---------------------------|-------|------------------|--|-------|------|------|
| | | | | Min. | Max. | |
| Read Cycle Time | | t _{RC} | — | 170 | — | ns |
| Address Cycle Time | | t _{ACC} | $\overline{CE}_x = V_{IH}, V_{IL}$ $\overline{OE} = V_{IL}$ | — | 170 | ns |
| Card Enable Access Time | | t _{CE} | $\overline{OE} = V_{IL}$ | — | 170 | ns |
| Output Enable Access Time | *1 | t _{OE} | $\overline{CE}_x = V_{IH}, V_{IL}$ | — | 75 | ns |
| Output Disable Time | *2 | t _{DF} | — | — | 60 | ns |
| Output Hold Time | | t _{OH} | $\overline{CE}_x = V_{IH}, V_{IL}$ $\overline{OE} = V_{IL}$ | 0 | — | ns |

Notes: *1. The maximum delay of \overline{OE} is $t_{ACC} - t_{OE}$ within the ranges in which the t_{ACC} is not affected.*2. t_{DF} is determined by either \overline{CE}_x or \overline{OE} , whichever is faster with rise time.

The decision level is determined by the time the output is in a high-impedance state.

MB98A51121/51221/51321/51421/51521-17

3. Input/output Terminal Capacitance

($V_{IN}, V_{OUT} = GND$, $f = 1$ MHz, $T_A = +25^\circ C$)

| Parameter | Notes | Symbol | Value | | Unit |
|-----------------------------|-------|-----------|-------|------|------|
| | | | Min. | Max. | |
| Input Terminal Capacitance | *1 | C_{IN} | — | 75 | pF |
| Output Terminal Capacitance | *2 | $C_{I/O}$ | — | 50 | pF |

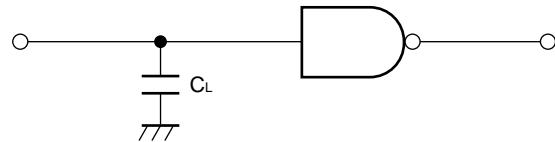
Notes: *1. Excluding \overline{CE}_1 and \overline{CE}_2 pins.

*2. Excluding WP, BVD1, BVD2, \overline{CD}_1 , and \overline{CD}_2 pins.

4. AC Characteristics Test Conditions

| | | |
|--------------------------------------|----------|------------------------------------|
| Input voltage | : | $V_{IH} = 2.6$ V, $V_{IL} = 0.6$ V |
| Input pulse rise time, fall time | : | $t_r, t_f = 5$ ns (0.8 V to 2.4 V) |
| Timing measurement reference voltage | : Input | $V_{IH} = 2.4$ V |
| | : Output | $V_{IL} = 0.8$ V |
| | | $V_{OH} = 2.2$ V |
| | | $V_{OL} = 0.8$ V |
| Output load | | : TTL + C_L (100 pF) |

• Output load circuit

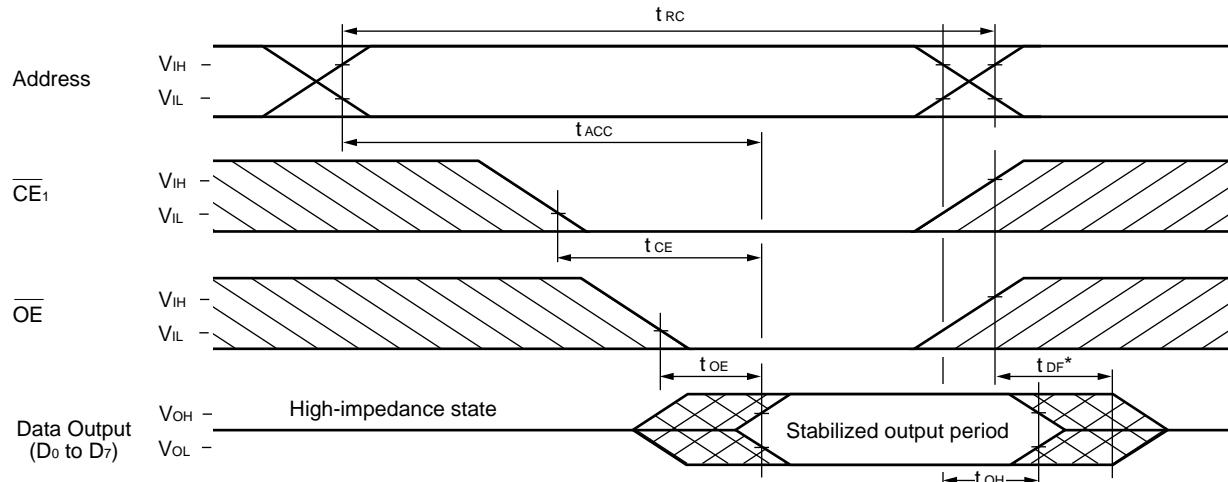


MB98A51121/51221/51321/51421/51521-17

■ TIMING DIAGRAM

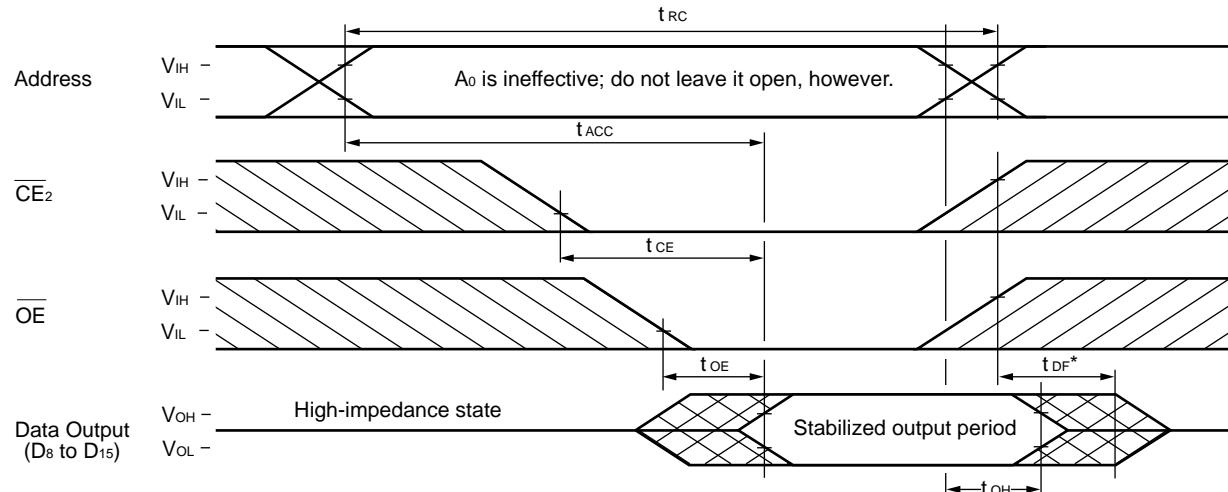
1. Common Memory Read Cycle

$\times 8$ bit ($\overline{CE}_2 = V_{IH}$)



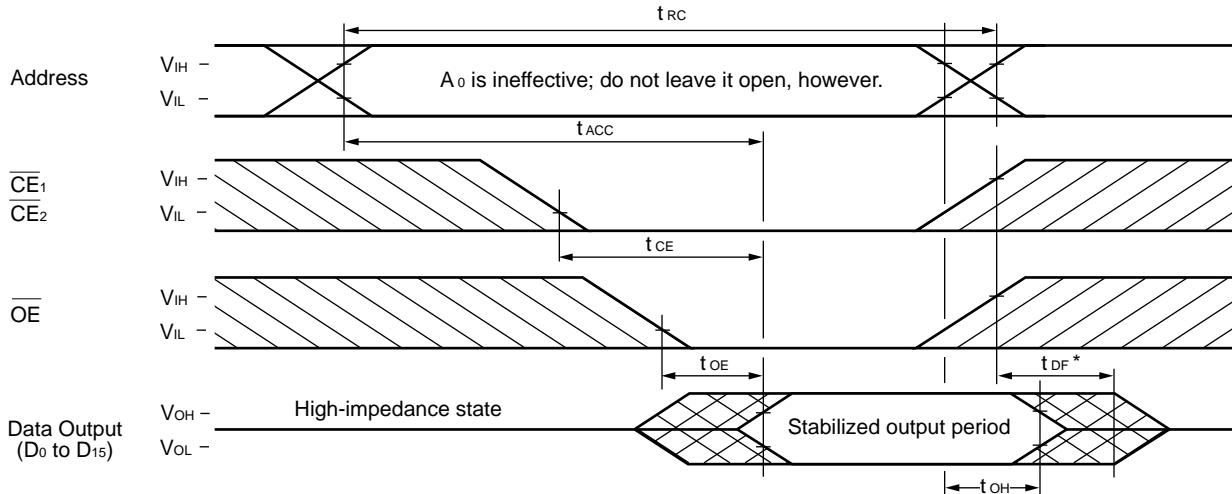
*: t_{DF} is determined by either \overline{OE} or \overline{CE}_1 , whichever is faster with rise time.
The decision level is determined by the time the output is in a high-impedance state.

$\times 8$ bit ($\overline{CE}_1 = V_{IH}$)



*: t_{DF} is determined by either \overline{OE} or \overline{CE}_2 , whichever is faster with rise time.
The decision level is determined by the time the output is in a high-impedance state.

(Continued)

MB98A51121/51221/51321/51421/51521-17*(Continued)* $\times 16$ bit (\overline{CE}_1 \overline{CE}_2)

*: t_{DF} is determined by either \overline{OE} or $\overline{CE}_1 = \overline{CE}_2$, whichever is faster with rise time.
 The decision level is determined by the time the output is in a high-impedance state.

MB98A51121/51221/51321/51421/51521-17

■ DATA RELEASE METHOD

Data release is accepted by the 8-Mbit EPROM (1 Mword × 8 bits).

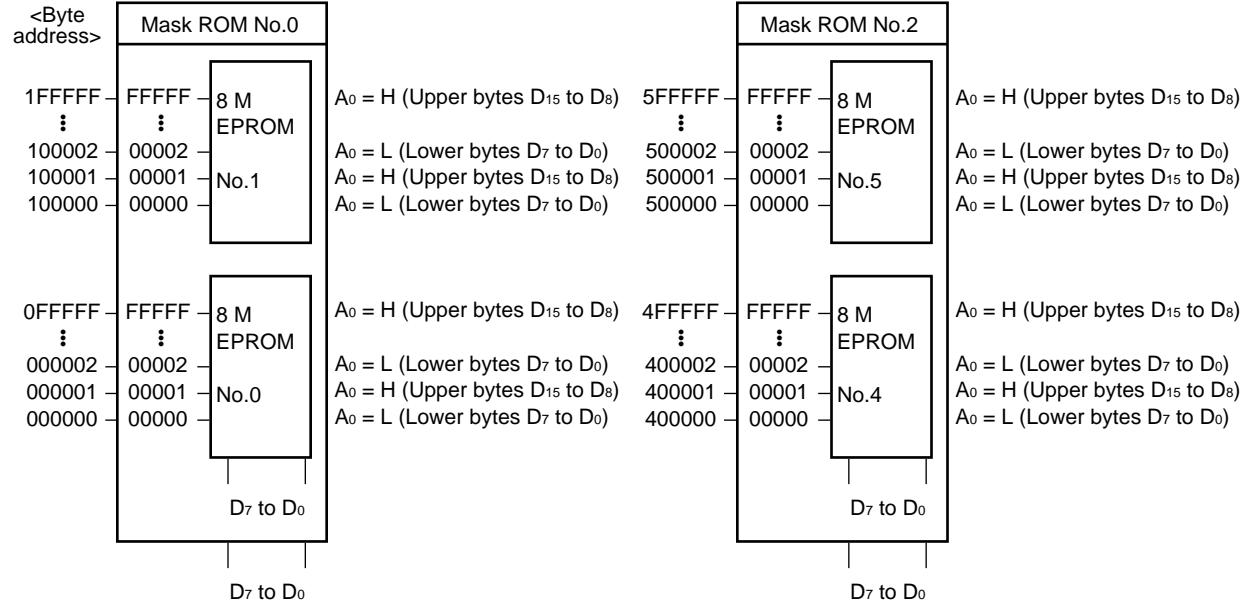
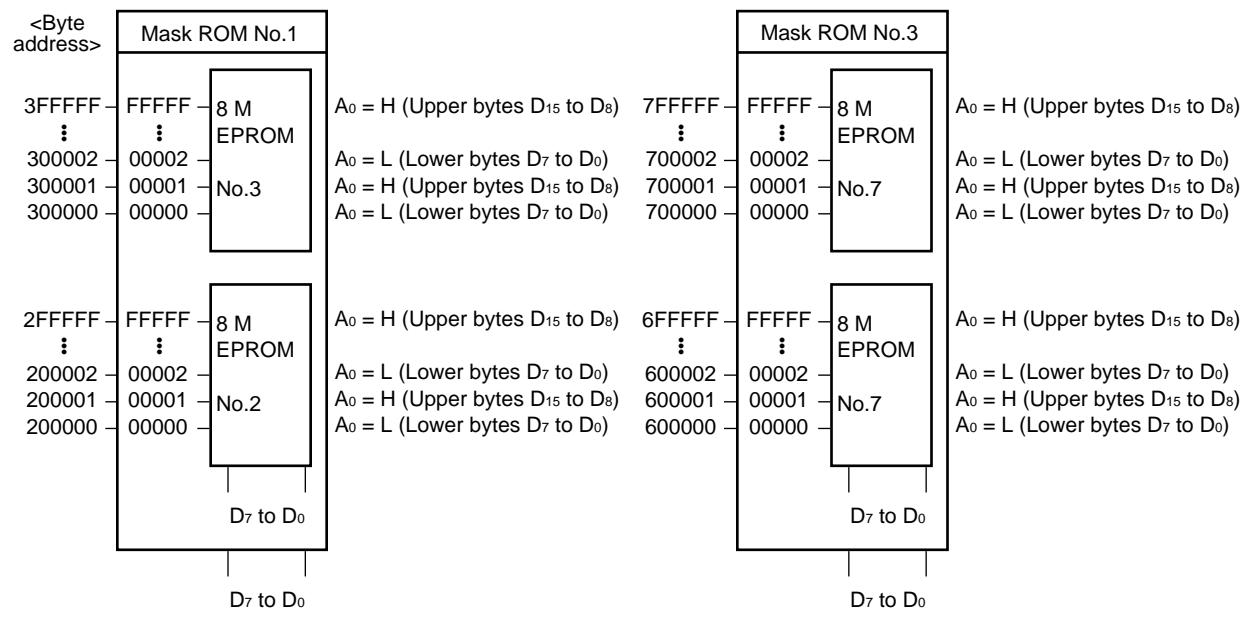
To prevent erroneous writing of data, provide three samples per piece of data. Also indicate the card memory address for writing.

- Mapping between release data EPROM address and memory card address
(16 Mbit Mask ROM × 1/ × 2/ × 4 being mounted)

The range of the address for the MB98A51121 is 000000 to 1FFFFFF (2 Mbytes).

The range of the address for the MB98A51221 is 000000 to 3FFFFFF (4 Mbytes).

The range of the address for the MB98A51321 is 000000 to 7FFFFFF (8 Mbytes).

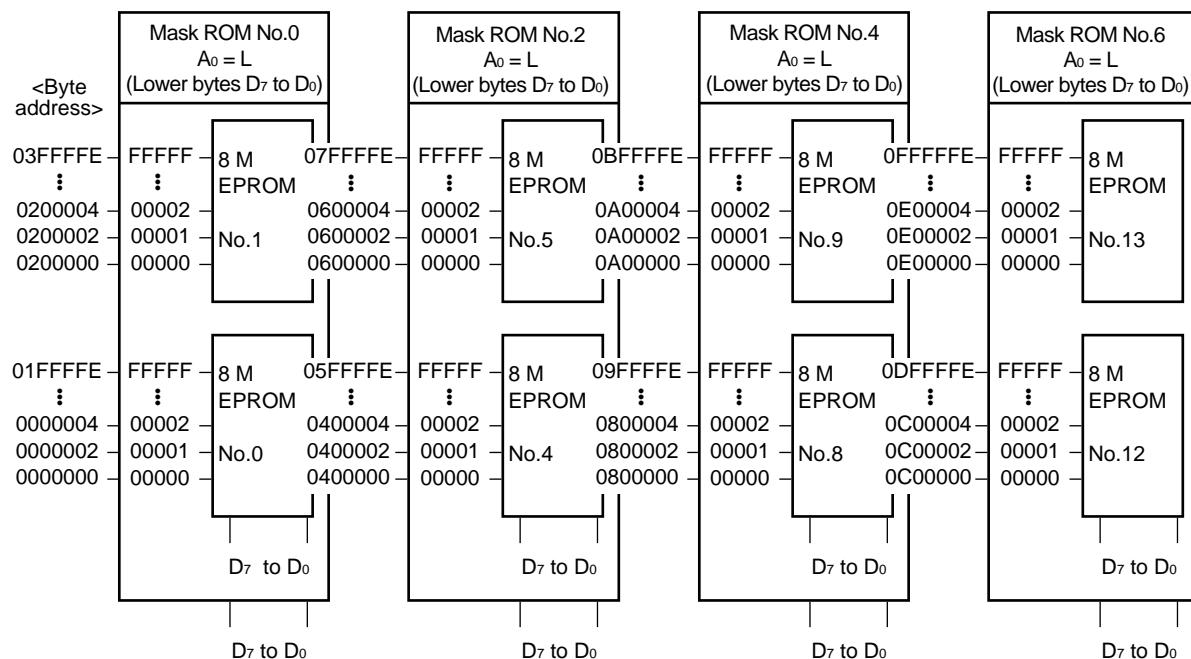
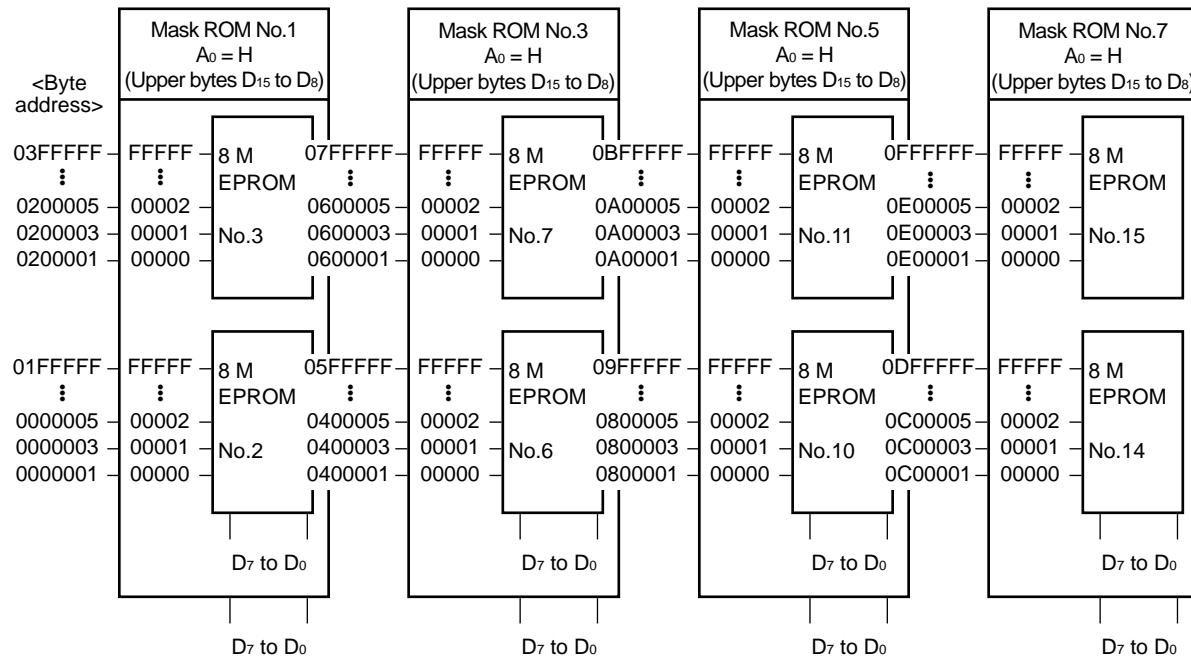


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MB98A51121/51221/51321/51421/51521-17

- Mapping between release data EPROM address and memory card address
(16 Mbit Mask ROM \times 8/ \times 16 being mounted)

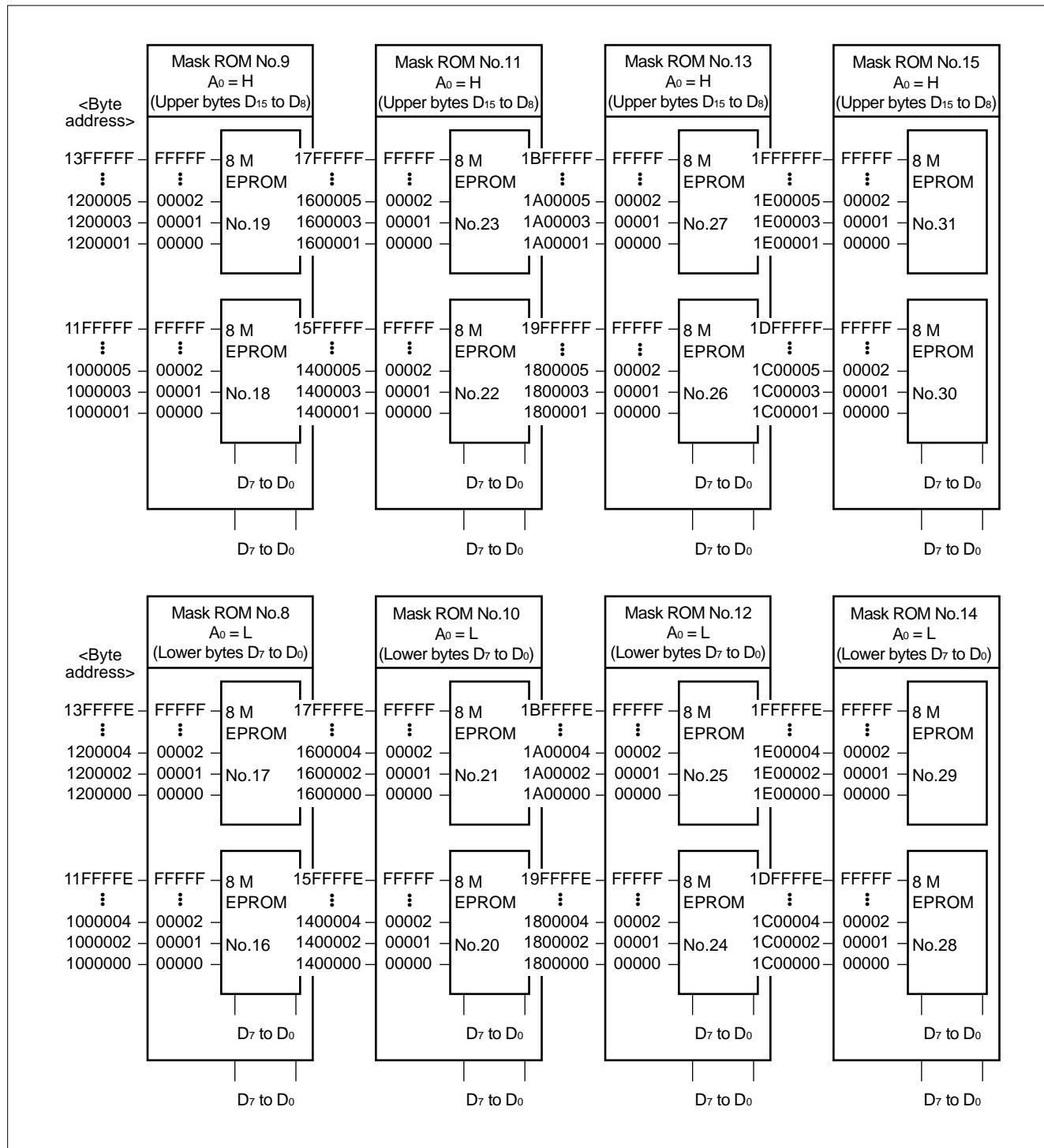
The range of the address for the MB98A51421 is 000000 to FFFFFFF (16 Mbytes).
The range of the address for the MB98A51521 is 0000000 to 1FFFFFF (32 Mbytes)



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MB98A51121/51221/51321/51421/51521-17

(Continued)



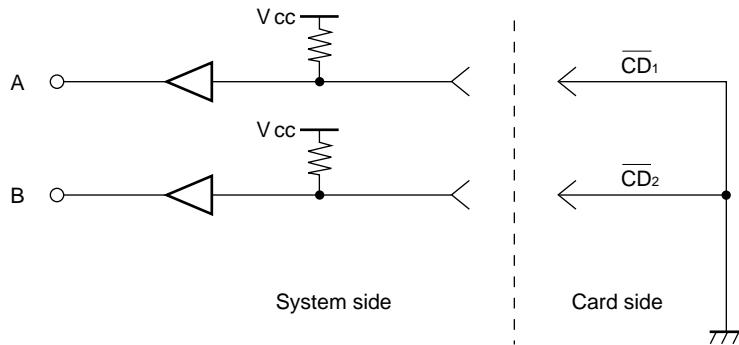
MB98A51121/51221/51321/51421/51521-17

■ AUXILIARY CAPABILITIES

1. Card Detection Pins (\overline{CD}_1 , \overline{CD}_2)

These pins verify a card is correctly inserted into the system.

The two pins are internally connected to the ground; with the system side connection being pulled up to the V_{CC} , detection of the voltage of these pins allows the system to check the state of connectivity of a card (See the diagram below).



2. Write Protection Pin (WP)

The Mask ROM Card, whose common memory is write-protected, outputs a high-level write-protection signal.

MB98A51121/51221/51321/51421/51521-17

■ DEVICE HANDLING PRECAUTIONS

The device is composed of fine electronic parts, so take care in handling or keeping it as below.

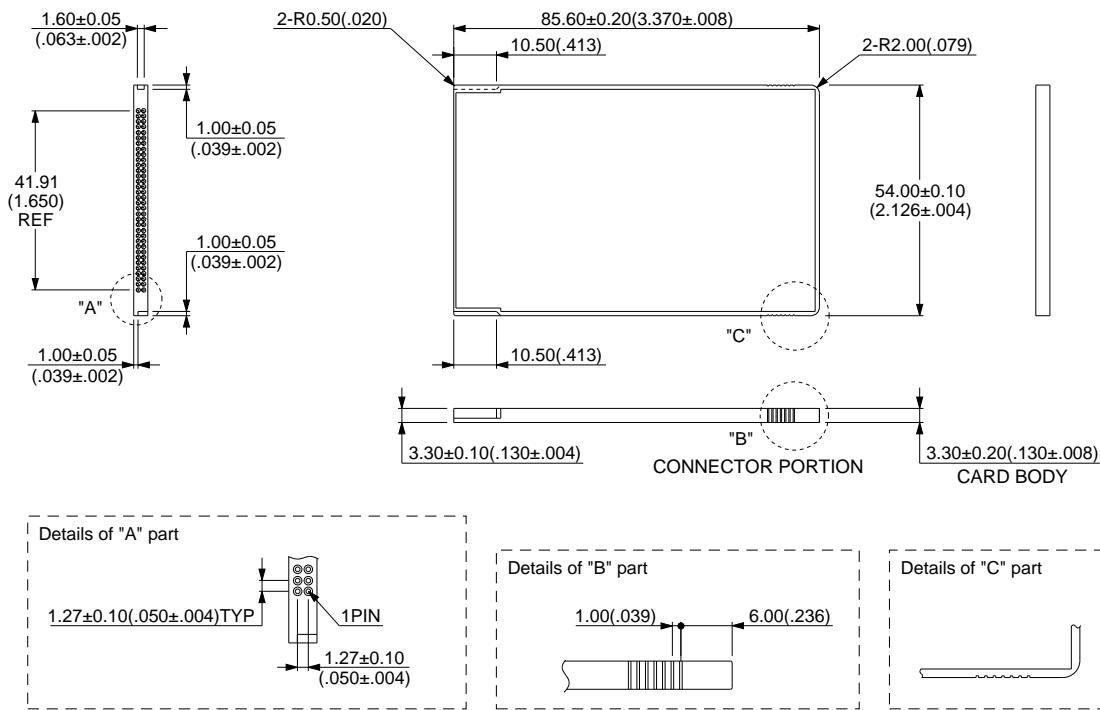
- The card is made fine, so do not keep it in the high temperature nor high humidity, place it in the direct sunlight nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken apart. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

MB98A51121/51221/51321/51421/51521-17

■ PACKAGE DIMENSIONS

68-pin Memory Card (CRD-68P-M02)

Note: Dimensions conform with PCMCIA/JEIDA



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Dimensions in mm (inches)

FUJITSU LIMITED

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